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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, LINH M	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/819,626	Applicant(s) LEVER, ANDREW M.	
	Examiner Linh M. Nguyen	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-4,8,23 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is a response to the Applicant's amendment submitted on 4/25/2002.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-4, 8, and 23-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Arcus (U.S. Patent No. 6,124,741).

With respect to claims 1, 3, 23, and 24, Figure 9 of Arcus shows a charge pump circuit and a corresponding operating method comprising 1) a first plurality of serially connected transistors [22,24] of a first conductivity type; 2) a second plurality of serially connected transistors [26,28] of a second conductivity type; 3) the first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; 4) the interconnection of the first and second plurality of transistors providing an output [VCTL]; wherein a) a gate of one of the first plurality of transistors [22] is adapted to receive a DOWN pulse signal [PD], b) a gate of another one of the first plurality of transistors [24] is adapted to receive a DC bias signal [BIASP], c) a gate of one of the second plurality of transistors [28] is adapted to receive an UP pulse signal [PDB], and d) a gate of the other of the second plurality of transistors [26] is adapted to receive another DC bias signal [BIASN]; and 5) a first node [36] at

the interconnection of the transistors of the first plurality of transistors being adapted to receive a DOWN pulse signal [Vpsrc], and a second node [38] at the interconnection of the transistors of the second plurality of transistors being adapted to receive an UP pulse signal [Vnsrc]. Fig. 9 of Arcus further shows a first capacitor circuit [44] for coupling the DOWN pulse signal to the first node [36], and a second capacitor [49] for coupling the UP pulse signal to the second node [38].

With respect to claim 2, Fig. 9 of Arcus discloses that the first plurality of transistors [22,24] are p-channel transistors, and the second plurality of transistors [26,28] are n-channel transistors.

With respect to claim 4, Fig. 9 of Arcus discloses that the first plurality of transistors [22, 24] is a pair of transistors, and the second plurality of transistors [26,28] is a pair of transistors.

With respect to claim 8, Fig. 9 of Arcus discloses a charge pump circuit comprising 1) a first plurality of serially connected transistors [22, 24] of a first conductivity type; 2) a second plurality of serially connected transistors [26,28] of a second conductivity type; 3) the first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; 4) the interconnection of the first and second plurality of transistors providing an output [Vctl]; wherein a) a gate of one of the first plurality of transistors [22] is adapted to receive a first switching signal [PD], b) a gate of another one of the first plurality of transistors [24] is adapted to receive a DC bias signal [BIASP], c) a gate of one of the second plurality of transistors [28] is adapted to receive a second switching signal [PDB], and d) a gate of the other of the second plurality of transistors [26] is adapted to receive another DC bias signal [BIASN]; and 5) a first node [36] at the interconnection of the transistors of the first plurality of transistors being adapted to receive a complementary first switching signal [Vpsrc],

and a second node [38] at the interconnection of the transistors of the second plurality of transistors being adapted to receive a complementary second switching signal [Vnsrc].

Remarks and Conclusion

3. Applicant's arguments submitted on 4/25/2002 have been fully considered but they are not persuasive.

With respect to the Applicant's argument on claim 1, in the second paragraph of page 5, the Applicant stated "the application of power-down and inverse power-down signals of Arcus would render the claimed invention inoperative". The Examiner disagrees. As shown in Fig. 9 of Arcus, the signals PD and PDB are applied to transistors [22 and 28], respectively, for turning them on. The function of these signals is similar to that of the DOWN\ and UP signals of the claimed invention in regard to the transistors P1 and N1.

With respect to the Applicant's argument on claim 8, in the second paragraph of page 6, the Applicant stated that Arcus does not teach or suggest "a first node at the interconnection of transistors of the first plurality of transistors to receive a complementary first switching signal and a second node at the interconnection of transistors of the second plurality of transistors to receive a complementary second switching signal". The Examiner disagrees. As clearly shown in Fig. 9 of Arcus, a first node [36] at the interconnection of the transistors of the first plurality of transistors is adapted to receive a complementary first switching signal [Vpsrc], and a second node [38] at the interconnection of the transistors of the second plurality of transistors is adapted to receive a complementary second switching signal [Vnsrc].

With respect to the Applicant's argument on claim 3, in the last paragraph of page 6 and the first paragraph of page 7, and related argument on claims 23-24 in the second paragraph of

page 7, the Examiner acknowledges that Arcus does not disclose a direct connection as shown in Fig. 4 of the claimed invention. However, based on the claimed language, figure 9 of Arcus reads all of the claimed subject matter in the claim 3. Arcus discloses, in Fig. 9, a first capacitor [44] for coupling the DOWN pulse signal to the first node, and a second capacitor [49] circuit for coupling the UP pulse signal to the second node; as such, all relevant steps claimed in claims 23-24 are contained therein (see 102(e) rejections above).

Consequently, all the claims remain anticipatory rejected by the teachings of Arcus (U.S. Patent No. 6,124,741).

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen

TIMOTHY P CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800